# Results of Single-Event Effects Measurements Conducted by the Jet Propulsion Laboratory

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Abstract— This paper reports recent single-event effects results for a variety of microelectronic devices that include an ADC, DAC, supervisory circuit, FIFO and a Viterbi decoder. The data was collected to evaluate these devices for possible use in NASA spacecraft.

Index Terms - Cyclotron, heavy ion, SEE, Latchup

#### I. INTRODUCTION

N recent years there has been increased interest in the possible use of unhardened commercial-off-the-shelf (COTS) electronic devices in space. They offer cutting-edge technology in terms of storage density, speed, and have superior electrical performance compared to hardened devices. However, unhardened COTS devices are susceptible to upset and degradation from radiation and therefore more information is needed on how they respond to radiation exposure before they can be safely used in space. The main method to study the reliability of a device is to measure its single-event effect (SEE) cross section as a function of ionizing power of the ion beam. In SEE measurements, the device under test (DUT) was monitored for soft errors, such as single event upset (SEUs) and for hard errors, such as single event latchup (SELs). SEE results for space applications have been published previously [1-4].

The studies discussed in this paper were undertaken to establish the sensitivity of the electronic devices to SEL and SEU. SEE measurements were performed on 5 different types of CMOS devices including ADC's, supervisory circuits, FIFO memory, and a Viterbi decoder.

#### II. EXPERIMENTAL PROCEDURE

## A Test Facilities

Heavy ion SEU measurements were performed at the Radiation Effects Facility located at the Cyclotron Institute

Manuscript received July 17, 2006. The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA).

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Texas A&M University (TAM). The TAM facility uses an 88" Cyclotron and provides a variety of ions beams over a range of energies for testing. Ion beams used in our measurements are listed in Table I. LET and range values are for normally incident ions. Test boards containing the device under test (DUT) were mounted to the facility test frame. Tests were done in air with normal incident beam. The tests at the TAM facility can be done in air because the higher energy ions available at this facility.

Table I. List of the ion beams used in our measurements at the TAM facility.

Ion	Energy	LET	Range
	(MeV)	(MeV-cm <sup>2</sup> /mg)	(µm)
$Ar^{40}$	519	8.5	186
Cu <sup>63</sup>	757	19.9	129
Kr <sup>84</sup>	1886	20.4	290
Xe <sup>129</sup>	2814	40.3	244
Ho <sup>165</sup>	1808	70.0	114
$Au^{197}$	2127	86.3	112

## **B** Experimental Methods

In general, the SEL test setup consisted of a computer, power supplies, and test boards specially designed for the device to be tested. A computer-controlled HP6629A power supply provides precision voltage control, current monitoring and latchup protection. Single event latchups were detected via the test system software. The software controls the power supply voltage, and monitors the supply current. The software also provides a strip chart of power supply measurements. In some cases, a separate computer was used to monitor the functionality of the test device.

DUT were tested at room temperature as well as an elevated temperature. The actual elevated temperature depended on the DUT specification [5]. To determine each cross-section point, either a minimum of fifty latchup events were accumulated or a beam fluence of 10<sup>7</sup>/ions/cm<sup>2</sup> was used.

The SEE evaluation included the measurements of saturation cross sections and the Linear Energy Transfer (LET<sub>th</sub>) threshold. The LET<sub>th</sub> is the minimum LET value necessary to cause a SEE at a fluence of  $1 \times 10^7$  ions/cm<sup>2</sup>.

#### III. TEST RESULTS AND DISCUSSION

#### 1) AD7714

The Analog Devices AD7714 is a 3/5 V, 500  $\mu A$  signal conditioning ADC. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance.

An evaluation board manufactured by Analog Devices was used for the test.

Two devices were tested at room temperature and at 85°C. At room temperature, the latchup threshold is below LET of 27 MeV-cm<sup>2</sup>/mg. At 85°C, the latchup threshold is below LET of 19 MeV-cm<sup>2</sup>/mg.

Figure 1 compares the result of room temperature measurements with that of the heated measurements. There was a factor of 1.5 -2.0 increase in the latchup cross section for the heated device.

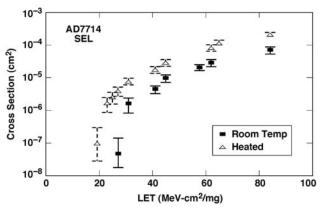


Figure 1. Comparison of latchup cross section at room temperature and 85°C for AD7714.

Previously, SEL and SEU measurements were performed on the AD7714 at BNL facility [6]. In these measurements two devices (different date code) were tested. The cross section measured in this work for SEU was about an order of magnitude lower than the cross section for SEL, a very unusual result. Somewhat surprisingly, the latchup cross section that we measured was nearly an order of magnitude lower than their measurement. This may be due to processing changes or "die shrinks" but is also possible that their measurement has overestimated the SEL cross section, perhaps because of excessive heating (tests at Brookhaven must be done in a vacuum chamber, and latchup is very sensitive to temperature) [5].

The AD7714 was tested for destructive latchup by turning off latchup protection. When the device went into a latchup state, the supply current increased to 1.2A. The lack of an output signal from the device indicated that the device was not functioning in this high current state. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did not recover, after power cycling, indicating that device had destructively failed.

Latchup rates for the AD7714 are calculated for interplanetary space GCR. The interplanetary space

environment is taken to be during solar minimum (worst case for GCR) and behind 100 mils of aluminum (but GCR rates are insensitive to spacecraft shielding).

A Weibull fit is combined with assumptions regarding directional effects to produce rate estimates for the stated environment. Directional effects were not measured, so two models are used to obtain two rate estimates for the environment. One is the Best Estimate model for directional effects, which is a guess that is probably close to reality but is not guaranteed. The other is the Worst Case model for directional effects, which is recommended for design purposes [7]. The rate estimates are presented in table II.

Table II. AD7714 Latchup Rate (per Device) from GCR

Environment	Best Estimate Rate	Worst Case Rate	
Inter. space (solar min. GCR)	1.5×10 <sup>-3</sup> /year	1.2×10 <sup>-2</sup> /year	

# 2) LTC1604

The Linear Technology LTC1604 is a 333ksps, 16-bit Analog to Digital Converter, (ADC) that draws 220mW from ±5V supplies.

The SEL measurements on devices from date code 8655, 8656 and 8659 were performed at TAM. The parts were tested at room temperature and at 85°C. Two parts from each date code were tested. This part has been tested for latchup previously [3]. However, the latchup LET threshold was not identified because of time constraints at TAM.

At room temperature SELs were observed at a LET of 65 MeV-cm<sup>2</sup>/mg but no latchups were observed at a LET of 63 MeV-cm<sup>2</sup>/mg. The latchup LET threshold is between 63 and 65 MeV-cm<sup>2</sup>/mg at room temperature. At elevated temperature of 85°C SELs were observed at LET of 58 MeVcm<sup>2</sup>/mg but no latchups were observed at a LET of 55 MeVcm<sup>2</sup>/mg. Our measurement did not show any date code dependency and there is a good agreement between measurements for devices from different lots. However, these date codes indicate that the parts were fabricated over a fiveweek period, so the conclusion about lot dependency may not be valid. Also, there is a good agreement between these measurements and results from Ref. [3]. In figure 2, we compare the result of room temperature measurements with that of the heated measurements. As one might expect, the latchup cross section is higher for the heated device.

Our latchup measurements indicate that LTC1604 is not highly sensitive to latchup. The cross section is relatively small, and rises to about 10<sup>-6</sup> at high LETs. The LTC1604 was tested for destructive latchup by turning off the current limit on the power supply. When the device went into a latchup state, the supply current increased to 600 mA. The lack of an output signal from the device indicated that the device was not functioning in this high current state. To determine if this

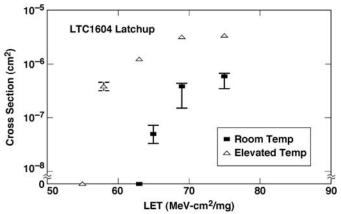


Figure 2. Comparison of latchup cross section at room temperature and 85°C for LTC1604.

condition was recoverable, the beam was turned off and the device was power cycled. The device did not recover, after power cycling, indicating that device had destructively failed.

Latchup rates for the LTC1604 are calculated for interplanetary space GCR. The interplanetary space environment is taken to be during solar minimum (worst case for GCR) and behind 100 mils of aluminum.

A Weibull fit is combined with assumptions regarding directional effects to produce rate estimates for the stated environment. The GCR rate estimate for best estimate and worst case are presented in table III.

Table III. LTC1604 Latchup Rate (per Device) from GCR

Environment	Best Estimate Rate	Worst Case Rate	
Inter. space (solar min. GCR)	2.6×10 <sup>-5</sup> /year	1.9×10 <sup>-4</sup> /year	

# 3) AD977

The Analog Devices AD977 is a 200 ksps, high speed, low power 16-bit ADC that operates from 5V supply.

An Evaluation board provided by manufacturer was used to test the device. The evaluation board required four power supplies and an analog input signal. The serial output from the AD977 was converted to parallel output by using two shift registers. A parallel DAC was used to convert the parallel output to an analog signal that was monitored with an oscilloscope.

An HP6629 quad power supply was used to power the AD977 test circuit. All four of the available supplies were used, one supply for Vdigital, one supply for Vanalog, and two supplies for the ± 15V required by the evaluation board support circuits. The AD977 ADC was tested for SEL. Two devices were tested at room temperature and one device was tested at both room temperature as well as an elevated temperature of 85°C. No latchups were observed for either the heated or the non-heated devices.

# 4) MAX708

The Maxim MAX708 is a microprocessor supervisory circuit. The MAX708 reduces the complexity and number of components required to monitor power-supply and battery functions in a microprocessor systems.

A printed circuit board was fabricated to provide the necessary supply voltages, input signals, and provision for monitoring the output signal. Two devices were tested at room temperature and one of the two devices was also tested at 125°C. At room temperature, the latchup threshold is between LET of 72 and 75 MeV-cm²/mg. For the heated device latchup threshold is below LET of 68 MeV-cm²/mg.

In figure 3, we compare the result of room temperature measurements with that of the heated measurements. As one might expect, the latchup cross section is higher for the heated device. There is a factor of about 10 increases in latchup cross section for the heated device. There is also a shift in the LET threshold towards lower LETs. This data indicates that, at room temperature, MAX708 is not highly sensitive to latchup. The cross section is relatively small, and rises to about  $5x10^{-7}$ cm<sup>2</sup> at high LETs (saturation cross section).

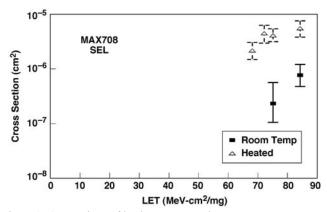


Figure 3. Comparison of latchup cross section at room temperature and 125°C for MAX708.

The MAX708 was tested for destructive latchup by turning off latchup protection. When the device went into a latchup state, the supply current increased to 415mA. The lack of an output signal from the device indicated that the device was not functioning in this high current state. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did recover, after power cycling, indicating that device had not been destructively failed.

A Weibull fit is combined with assumptions regarding directional effects to produce rate estimates for the stated environment. The GCR rate estimate for best estimate and worst case are presented in table IV.

Environment	Best Estimate Rate	Worst Case Rate	
Inter. space (solar min. GCR)	1.5×10 <sup>-5</sup> /year	1.1×10 <sup>-4</sup> /year	

Table IV. MAX708 Latchup Rate (per Device) from GCR

# 5) 72V36110

The IDT 72V36110 is a high speed, CMOS First-In-First-Out (FIFO) memories with clocked read and write controls and a flexible Bus-Matching x36/x18/x9 data flow.

A Spartan-IIE digital I/O development platform was used to provide the input patterns needed to write to the 72V36100 FIFO and was also used to read the patterns from the FIFO. Prior to heavy ion exposure, the FIFO memory was written to, using an alternating pattern, and during heavy ion exposure, the FIFO memory was read from and the output pattern compared to the pattern previously written into FIFO memory. This was done to monitor the device for upsets and also to monitor the device for functionality. An alternating pattern was used to provide addressing errors visibility.

A printed circuit board was fabricated to interface the Spartan-IIE digital I/O board to the test device. The 72V36110 was tested for SEU and SEL.

# 1- SEL Test Results

We performed latchup measurement on 72V36110 in two different mode of operation: static and dynamic. In static mode no read or write operation was performed during irradiation and simply memory cells were tested for latchup. On the other hand in dynamic mode memory cells were interrogated during irradiation and read and write circuit were also subject to latchup testing. Two devices were tested at room temperature as well as at an elevated temperature of 80°C. The elevated temperature measurements were done for only low LETs. At room temperature, SELs were observed at a LET of 8.2 MeV-cm<sup>2</sup>/mg but no latchups were observed at a LET of 5 MeV-cm<sup>2</sup>/mg. The latchup LET threshold is between 5 and 8.2 MeV-cm<sup>2</sup>/mg at room temperature. At elevated temperature of 80°C, SEL were observed at LET of 5 MeV-cm<sup>2</sup>/mg but no latchups were observed at a LET of 2.7 MeV-cm<sup>2</sup>/mg. The latchup LET threshold is between 2.7 and 5 MeV-cm<sup>2</sup>/mg at elevated temperature of 80°C. In figure 4, we compare the result of static and dynamic at room temperature measurements with that of the heated measurements.

There is a factor of about 100 increases in latchup cross section for the heated device. There is also a shift in the LET threshold towards lower LETs. These data indicates that, 72V36110 in highly sensitive to the latchup. The LET threshold is low and the cross section is large, and rises to about  $5x10^{-3}$  cm<sup>2</sup> at high LETs.

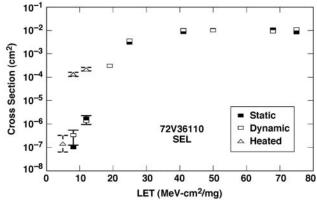


Figure 4. Comparison of SEL data obtained at room temperature with the heated measurement for 72V36110.

The 72V36110 was tested for destructive latchup by turning off latchup protection. When the device went into a latchup state, the supply current increased to 200mA. The lack of an output signal from the device indicated that the device was not functioning in this high current state. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did recover, after power cycling, indicating that device had not been destructively failed.

## 2- SEU Test Results

The setup used for latchup measurements was utilized to perform SEU testing at the same time. Devices with complex internal structure are rather difficult to test for a wide range of SEUs simultaneously. Given the constraints of the test development, and capabilities of the test system, the primary SEU result is the SRAM cell upset cross section. In order to do this SEU testing, the DUTs were exercised by a test program running on the soft-core Xilinx MicroBlaze processor.

In order to observe SRAM SEU events, the tester was used to write a pattern to the FIFO before irradiation, and the FIFO was read out after irradiation. Bit flips in the data stream are SRAM cell upsets. The SEU data is considered static because the upsets were correlated with the beam.

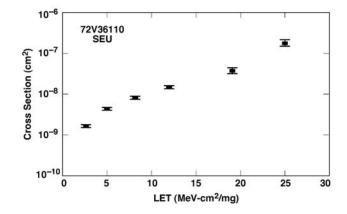


Figure 5. SEU cross section for IDT 72V36110.

Because of large contribution from latchup events it was impossible to perform SEU measurements at high LETs. The SEU measurement were done up to LET 25 MeV-cm<sup>2</sup>/mg. The LET threshold for SEU measurement was below 2.7 MeV-cm<sup>2</sup>/mg and the cross section at LET 25 MeV-cm<sup>2</sup>/mg was about 1.9x10<sup>-7</sup> cm<sup>2</sup>/bit. In Figure 5, we show results of SEU measurement. The device is very sensitive to SEU.

We note that previous SEE measurements of this device [8] provided similar results in terms of the SEU and SEL cross sections compared to our measurements.

#### 6) TSS902F

The ATMEL TSS902F is a forward error correction Viterbi decoder. The TSS902E is built on MG1RT CMOS 0.6 µm Sea of Gates technology. MG1RT is a radiation tolerant process [9]. Test structure was built on an epitaxial substrate with increase in the n-well implantation dose, to decrease sensitivity to latchup.

The test structure heavy ions latchup sensitivity was characterized using different ions up to LET of 120 MeV-

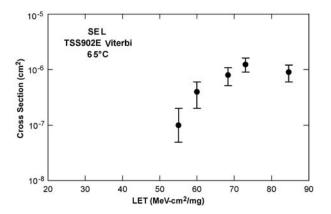


Figure 6. Latchup cross section at 65° C for TSS90E

At  $125^{\circ}$  C, also there is good agreement between latchup measurements of both devices. In Fig. 7, we show average result for two devices that were tested at  $125^{\circ}$  C. The error bars are  $\sim 1$  sigma and result from Poisson statistics. These data indicate that TSS902E is relatively sensitive to latchup and has an LET threshold below 41 MeV-cm²/mg. However, the cross section is relatively small at low LETs, gradually rising to about  $5 \times 10^{-6} \text{cm}^2$  at high LETs (saturation cross section).

cm<sup>2</sup>/mg. No latchup occurred during the irradiation [10]. The latchup tests were performed on the test structure only at room temperature and not at an elevated temperature. No latchup measurements were done on the chip itself.

A printed circuit board was fabricated to mount and bias the DUT during the radiation tests. The TSS902E was tested in a static condition.

SEL Measurements were performed at room temperature, at the application temperature of 65°C and at the maximum operating temperature specified by the manufacturer (125°C).

At room temperature no latchup event was observed up to an LET of 84.6 MeV-cm<sup>2</sup>/mg.

At 65° C latchups were observed at LET of 58 MeV-cm<sup>2</sup>/mg but no latchups were observed at LET 55 MeV-cm<sup>2</sup>/mg. Thus, at 65° C the latchup LET threshold is between 55 and 58 MeV-cm<sup>2</sup>/mg. At this temperature the latchup results for both devices were in good agreement. In Fig. 6, we show the average result of both 65° C measurements. The cross section is small and rises to about 10<sup>-6</sup>cm<sup>2</sup> at high LETs.

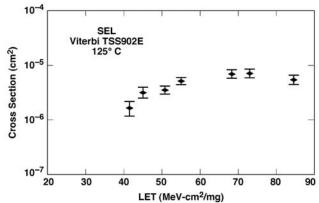


Figure 7. Latchup cross section at 125° C for TSS90E

#### IV. SUMMARY

Table V summarizes the SEE test results for the five devices included in this paper.

Table V. Summary of SEE test results.

Part Number	Manufacture	Device	Test Results
		Function	LET in MeV-cm <sup>2</sup> /mg; σ in cm <sup>2</sup> /device
AD7714	Analog	Serial 24-bit	SEL LET <sub>th</sub> $< 27$ ; $\sigma_{SAT} \sim 1 \times 10^{-6}$ , Destructive
	Devices	ADCs	
LTC1604	Analog	Serial 16-Bit	SEL LETth $> 63$ ; $\sigma_{SAT} \sim 5 \times 10^{-7}$ , Destructive
	Devices	ADCs	
AD977	Analog	Serial 16-Bit	$SEL LET_{th} > 84$
	Devices	ADCs	
MAX708	Maxim	μP Supervisory	SEL LET <sub>th</sub> $< 75$ ; $\sigma_{SAT} \sim 1 \times 10^{-6}$
		Circuit	
72V36110	IDT	FIFO Memory	SEL LET <sub>th</sub> $> 5$ ; $\sigma_{SAT} \sim 1 \times 10^{-2}$
			SEU LET <sub>th</sub> $< 2.7$
TSS902F	Atmel	Viterbi Decoder	SEL LETth $> 55$ ; $\sigma_{SAT} \sim 1 \times 10^{-6}$ at $65^{\circ}$ C

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